GSN Signal Assignments

for

Extended Shield Double Stack Receptacle

Board edge

"B" Section

	Signal	Pin	Pin	Signal	
nc	not used	B68	B34	D14_IN_P	L9
	not used	B67	B33	D14_IN_N	
L10	CLOCK_IN_P	B66	B32	C3_IN_P	R10
	CLOCK_IN_N	B65	B31	C3_IN_N	
	GND	B64	B30	GND	
L11	C0_IN_P	B63	B29	C1_IN_P	R11
	C0_IN_N	B62	B28	C1_IN_N	
	GND	B61	B27	GND	
R12	C2_IN_P	B60	B26	D15_IN_P	R9
	C2_IN_N	B59	B25	D15_IN_N	
	GND	B58	B24	GND	
L8	D12_IN_P	B57	B23	D13_IN_P	R8
	D12_IN_N	B56	B22	D13_IN_N	
	GND	B55	B21	GND	
R7	D11_IN_P	B54	B20	D10_IN_P	L7
	D11_IN_N	B53	B19	D10_IN_N	
	GND	B52	B18	GND	
	GND	B51	B17	GND	
	D11_OUT_N	B50	B16	D10_OUT_N	
	D11_OUT_P	B49	B15	D10_OUT_P	
	GND	B48	B14	GND	
	D12_OUT_N	B47	B13	D13_OUT_N	
	D12_OUT_P	B46	B12	D13_OUT_P	
	GND	B45	B11	GND	
	C2_OUT_N	B44	B10	D15_OUT_N	
	C2_OUT_P	B43	B9	D15_OUT_P	
	GND	B42	B8	GND	
	C0_OUT_N	B41	B7	C1_OUT_N	
	C0_OUT_P	B40	B6	C1_OUT_P	
	GND	B39	B5	GND	
	CLOCK_OUT_N	B38	B4	C3_OUT_N	
	CLOCK_OUT_P	B37	B3	C3_OUT_P	
	not used	B36	B2	D14_OUT_N	
	not used	B35	B1	D14_OUT_P	

"A" Section

	Signal	Pin	Pin	Signal	
L6	FRAME_IN_P	A1	A35	D09_IN_P	R6
	FRAME_IN_N	A2	A36	D09_IN_N	
R5	DO6_IN_P	A3	A37	DO8_IN_P	L5
	DO6_IN_N	A4	A38	DO8_IN_N	
	GND	A5	A39	GND	
L4	D07_IN_P	A6	A40	D04_IN_P	R4
	D07_IN_N	A7	A41	D04_IN_N	
	GND	A8	A42	GND	
R3	D03_IN_P	A9	A43	D05_IN_P	L3
	D03_IN_N	A10	A44	D05_IN_N	
	GND	A11	A45	GND	
L2	D02_IN_P	A12	A46	D01_IN_P	R2
	D02_IN_N	A13	A47	D01_IN_N	
	GND	A14	A48	GND	
R1	CLOCK_2_IN_P	A15	A49	D00_IN_P	L1
	CLOCK_2_IN_N	A16	A50	D00_IN_N	
	GND	A17	A51	GND	
	GND	A18	A52	GND	
	CLOCK_2_OUT_N	A19	A53	D00_OUT_N	
	CLOCK_2_OUT_P	A20	A54	D00_OUT_P	
	GND	A21	A55	GND	
	D02_OUT_N	A22	A56	D01_OUT_N	
	D02_OUT_P	A23	A57	D01_OUT_P	
	GND	A24	A58	GND	
	D03_OUT_N	A25	A59	D05_OUT_N	
	D03_OUT_P	A26	A60	D05_OUT_P	
	GND	A27	A61	GND	
	D07_OUT_N	A28	A62	D04_OUT_N	
	D07_OUT_P	A29	A63	D04_OUT_P	
	GND	A30	A64	GND	
	DO6_OUT_N	A31	A65	DO8_OUT_N	
	DO6_OUT_P	A32	A66	DO8_OUT_P	
	FRAME_OUT_N	A33	A67	D09_OUT_N	
	FRAME_OUT_P	A34	A68	D09_OUT_P	

SuMAC

Table 1

The table above illustrates the GSN signal assignment for the Extended Shield Double Stack Receptacle proposed by FCI-Berg. The pin numbers are per the current FCI drawing number 73692. Note that the "top" receptacle makes connection to the board farthest from the card edge and has been assigned pin numbers A1 through A68 as illustrated in table 1. The "bottom" receptacle makes connection to board closest to the board edge and has been assigned pin numbers B1 through B68 as illustrated in table 1.

Polarization concern: Due to the lack of polarization in the current receptacle, their has been some discussion about flipping the "d-shell" housing around in one of the two receptacles. FCI indicates that due to symmetry and modularity of the components of this connector, either d-shell could be reversed without effecting the rest of the connector. If the d-shell is reversed, as proposed, then the pin numbering for section B would flip, and thus be numbered exactly like the A section of the connector. Note that the signals listed in the table would still route to the same pin locations, only the numbering of those locations would change.

The signal assignment illustrated in table 1 is the result of several constraints:

First, all of the signals must be able to “escape” from the connector pin fields and route to circuitry on the interior of the circuit board. I assumed that only one trace is allowed between diagonal pins. This was by far the most limiting constraint for this connector as it contains 8 rows of contacts, were the previous connector contained 4 rows.

Second, anti-pads touch on diagonal pins, creating unwanted “slots” in the power and ground plans, so strategically located pins are connected to signal ground to provide ground paths through the connector pin fields for high frequency return paths. These same ground pins provide an extra measure of cross talk isolation between pairs as they travel through the connector assembly and into the mating connector. For EMI reasons, these signal grounds will stop at that point and will not be connected to any conductor in the cable assembly.

Third, I assumed that cable construction might include “quads” as in some of the current cables. Signals are aligned so as not to split quads between connector sections.

Fourth, the signals are assigned with a mirror image relationship between the input and output signals. This should aid in the splaying out of the cable on both ends and facilitate the use of coiled ribbon construction cables as well. As before, the “flip” required between the transmitting and receiving signals is in the cable.

Although splitting the signals so that inputs are in one section and outputs in the another section was deemed valuable goal, this assignment was impossible due to the different impedance’s on the card, and the amount of route crossing it would require on the board. Another disadvantage of that scheme, was the added complexity it would add to loop-back plugs and paddleboards.

In addition to the signal assignment, routing numbers for the input signals are indicated in the table as well. The input signals are the most difficult to route due to the fact that they should be routed as 150 differential pairs until they terminate near the SuMAC. This 150 differential requirement usually requires using multiple dielectric layers. Combining dielectric layers reduces the number of usable layers for this routing on a given thickness card. The card is assumed to be 0.0625” for compatibility with the PCI connector. It was assumed that only two layers may be available for the receive signals and the above signal assignment supports such a layout to the SuMAC. The routing strategy is illustrated in figure 1 below.

The numbers in table 1 proceeded by L or R, indicate the order that the signals should occupy the routing channels of the two layers. Signals preceded by L are to be routed on one layer, while signals proceeded by R are to be routed on the other layer. The number indicates the sequential routing lanes from bottom to top.

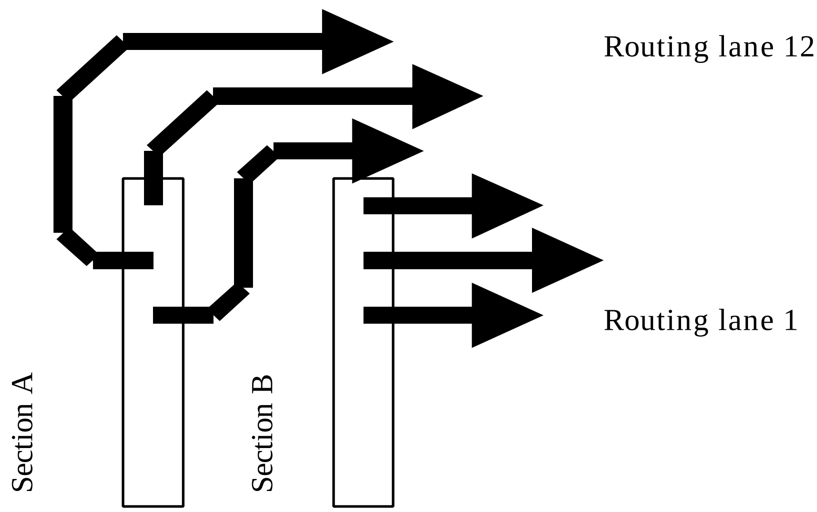

Figure 1