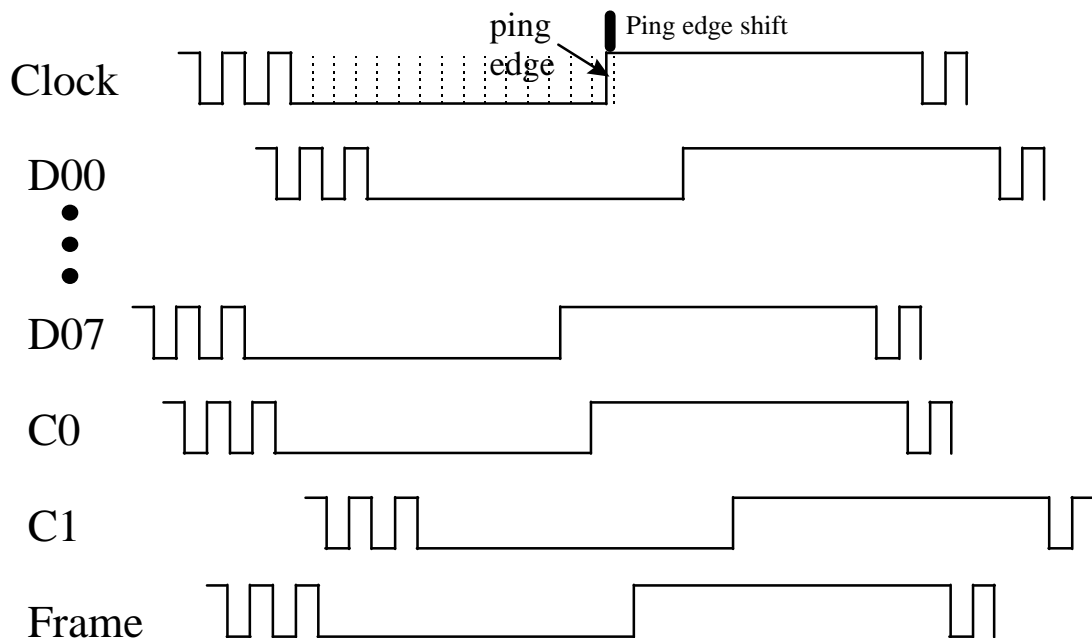


Note: This document is a rough draft on how jitter and skew should be allocated in the HIPPI-6400 parallel fiber optic data link. It is the output of a series of discussions amongst several members of the HIPPI-6400-Optical group (notably Dan Brown-AMP, Greg Chesson-SGI, Steve Joiner-HP, Schelto van Doorn-Siemens, and Mark Donhowe-Gore). At this time we would like to submit this document to the larger community to request feedback on our reasoning; we want to catch any oversights before going further into detail.

## HIPPI-6400-Optical Skew/Jitter Allocations

The HIPPI-6400-Opt parallel fiber optic data link consists of 12 parallel channels running in each direction at the nominal data rate of 1 Gb/s. Typically, the data, clock, and control signals will arrive at the destination skewed in time. A deskew training pattern is placed on all the signals in order to align (deskew) the signals. The training pattern is shown in Figure 1 (editor's note: check if it is the correct training pattern from HIPPI-6400-PH). Also depicted in Figure 1 is an example of the relative skew the signals could endure. The deskew circuitry in the HIPPI-6400 SuMAC chip uses the 'ping edge' to align the signals and then shifts the clock signal  $\frac{1}{4}$  period so as to center the clock transition to the center of the signal eye patterns. The ping edge is the transition in the middle of the training pattern. This training cycle is run at least every 10  $\mu$ s to adjust for drift.

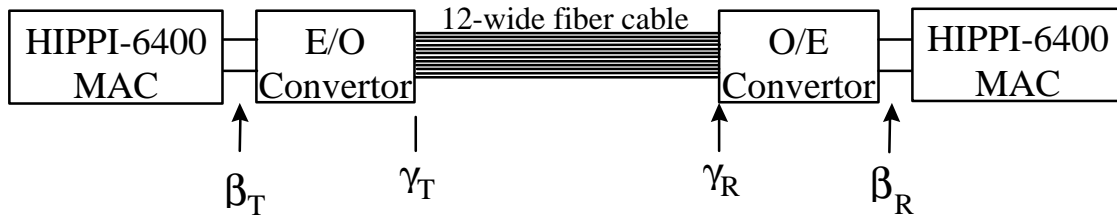


**Figure 1. Example of relative skew seen at destination with the training pattern that is used to deskew the signals**

Also shown in Figure 1 is the ping edge shift,  $\tau_{pes}$ . Normally the clock is a repeating 1 ns 'off' / 1 ns 'on' signal that has a repeatable clock transition time. The training pattern changes the clock to 14 ns 'off' / 14 ns 'on' which causes a shift in the expected transition time due to pattern dependent effects. This shift has been labeled 'ping edge shift' and must be accounted for in the timing budget.

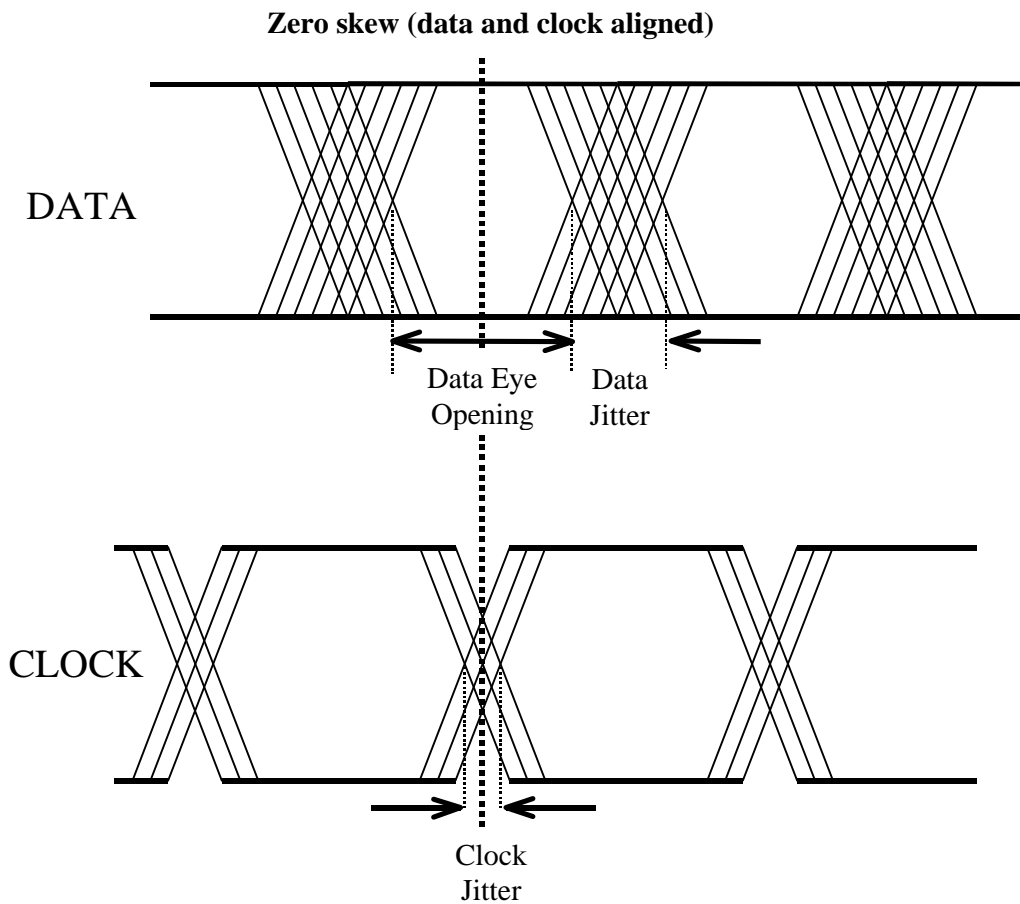
The circuitry causes two other timing effects. First, the SuMAC deskew circuitry uses delay line taps which work in discrete time slots; this means the data or clock transition edges can only be located within

the tap delay  $\tau_{\text{tap}}$ . Second, a set-up and hold time  $\tau_{\text{s\&h}}$  is required for the latch to operate. These timing effects plus the usual jitter budget allocations need to be accounted for in order to establish a realizable link. We can define jitter reference points as per Figure 2.



**Figure 2. HIPPI-6400-Opt parallel data link jitter reference points**

In Figure 2,  $\beta_T$  defines the jitter reference point at the interface between the HIPPI-6400 Media Access Controller (MAC) and the electrical input to the parallel fiber optic transmitter module.  $\gamma_T$  is the jitter reference point at the optical output of the transmitter module. Likewise,  $\gamma_R$  is the reference point at the optical input and  $\beta_R$  is the reference point at the electrical output of the parallel fiber optic receiver module. An aligned but otherwise typical (i.e., non-training cycle) clock and data signal eye pattern at the  $\beta_R$  reference point might appear as shown in Figure 3.



**Figure 3. Eye patterns of typical clock and data lines with zero skew at HIPPI-6400 MAC receiver input ( $\beta_R$ ) jitter reference point**

Conceptually, it can be seen from Figure 3 that the total clock jitter must be less than the data eye opening in order to make a valid decision. Specifically, the clock jitter  $TJ_{\text{clocktotal}}$  is the total jitter contributed by the clock channel and the data eye opening is the bit period (unit interval) minus the total jitter contributed by the data channel  $TJ_{\text{datatotal}}$ , both measured at the receiver electrical input to the HIPPI-6400 MAC ( $\beta_R$  jitter reference point):

$$TJ_{\text{clocktotal}} \leq 1 - TJ_{\text{datatotal}} = \text{data eye opening at } \beta_R \text{ (for a perfectly aligned system)}$$

Furthermore,

$$TJ_{\text{clocktotal}} = \text{MAC clock source jitter } TJ_{\text{clk}} + \text{clock optics jitter } TJ_{\text{opc}}$$

$$TJ_{\text{datatotal}} = \text{MAC data source jitter } TJ_{\text{dat}} + \text{data optics jitter } TJ_{\text{opd}}$$

Here, the HIPPI-6400 MAC clock and source channel jitter is measured at the  $\beta_T$  reference point. The clock line and data line optics jitter,  $TJ_{\text{opc}}$  and  $TJ_{\text{opd}}$ , is the total jitter contributed by the optics link ( $\beta_T$  to  $\beta_R$  points).

In addition, to properly align the skewed signals, a delay line tap placement accuracy ( $\tau_{\text{tap}}$  for clock placement accuracy plus  $\tau_{\text{tap}}$  for data placement accuracy) must be added to the setup and hold time  $\tau_{\text{s\&h}}$  and to the ping edge shift  $\tau_{\text{pes}}$ . Our equation is thus:

$$TJ_{\text{clk}} + TJ_{\text{dat}} + TJ_{\text{opc}} + TJ_{\text{opd}} + \tau_{\text{pes}} + 2\tau_{\text{tap}} + \tau_{\text{s\&h}} \leq 1 \text{ UI} = 1 \text{ ns.}$$

The initial estimate of numbers produced the following table. The next step is to verify these numbers (and perhaps expand the table).

**Table 1. Jitter component allocations**

Parameter	Symbol	Typical	Units	Comments
Clock source jitter	$TJ_{\text{clk}}$	32	ps	Total jitter contributed by SuMAC source on clock line ( $\beta_T$ point).
Data source jitter	$TJ_{\text{dat}}$	32	ps	Total jitter contributed by SuMAC source on data and other non-clock lines ( $\beta_T$ point).
Clock optics jitter	$TJ_{\text{opc}}$	230	ps	Total jitter contributed by the optics link on clock lines ( $\beta_T$ to $\beta_R$ ).
Data optics jitter	$TJ_{\text{opd}}$	380	ps	Total jitter contributed by the optics line on data and other non-clock lines ( $\beta_T$ to $\beta_R$ ).
Ping edge shift	$\tau_{\text{pes}}$	80	ps	The shift in time of the clock transition as a result of the training cycle timing pattern.
2X tap delay time	$2\tau_{\text{tap}}$	160	ps	$2\tau_{\text{tap}}$ is the clock misalignment due to the discrete tapped delay time placement $\tau_{\text{tap}}$ of the SuMAC deskew circuitry.
Setup an hold time	$\tau_{\text{s\&h}}$	83	ps	Setup and hold time required for SuMAC latch to operate.
<b>SUM</b>		997	<b>ps</b>	<b>Last Equation</b>